

FIG. 1

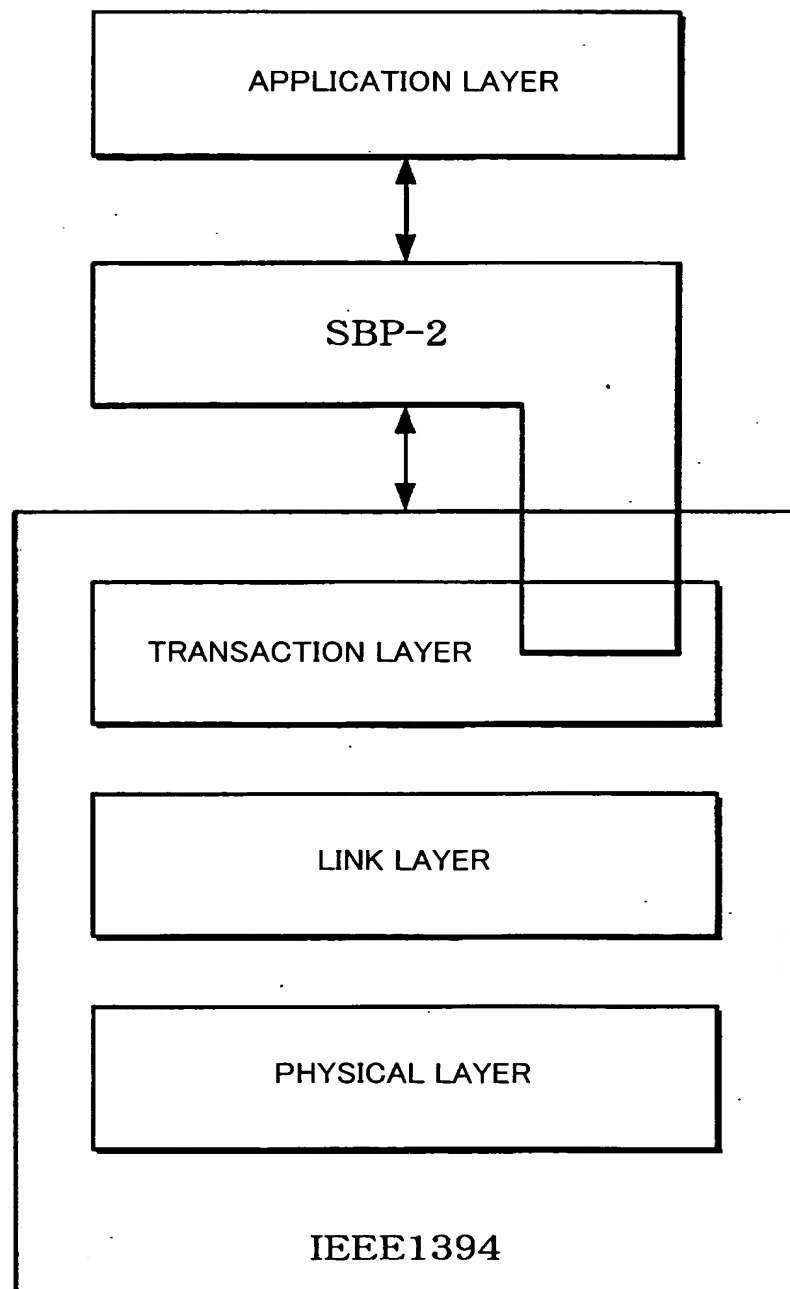


FIG. 2

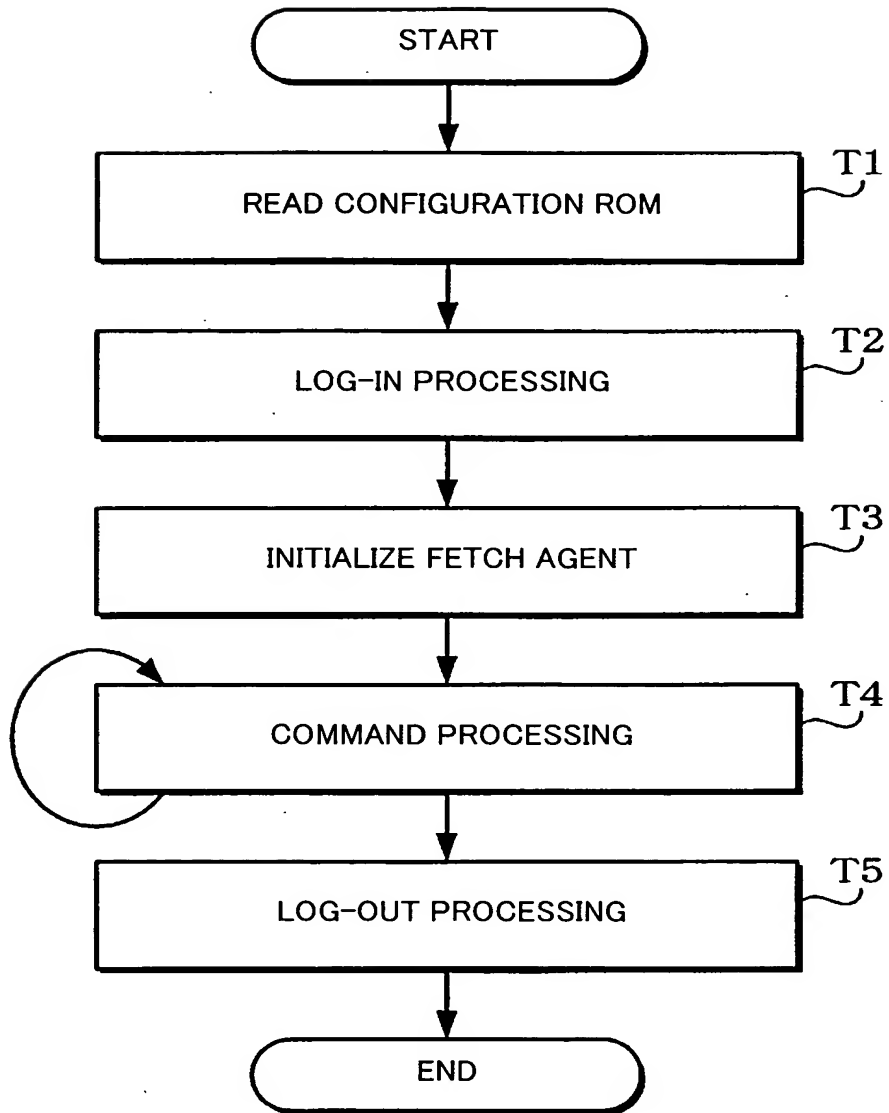


FIG. 3

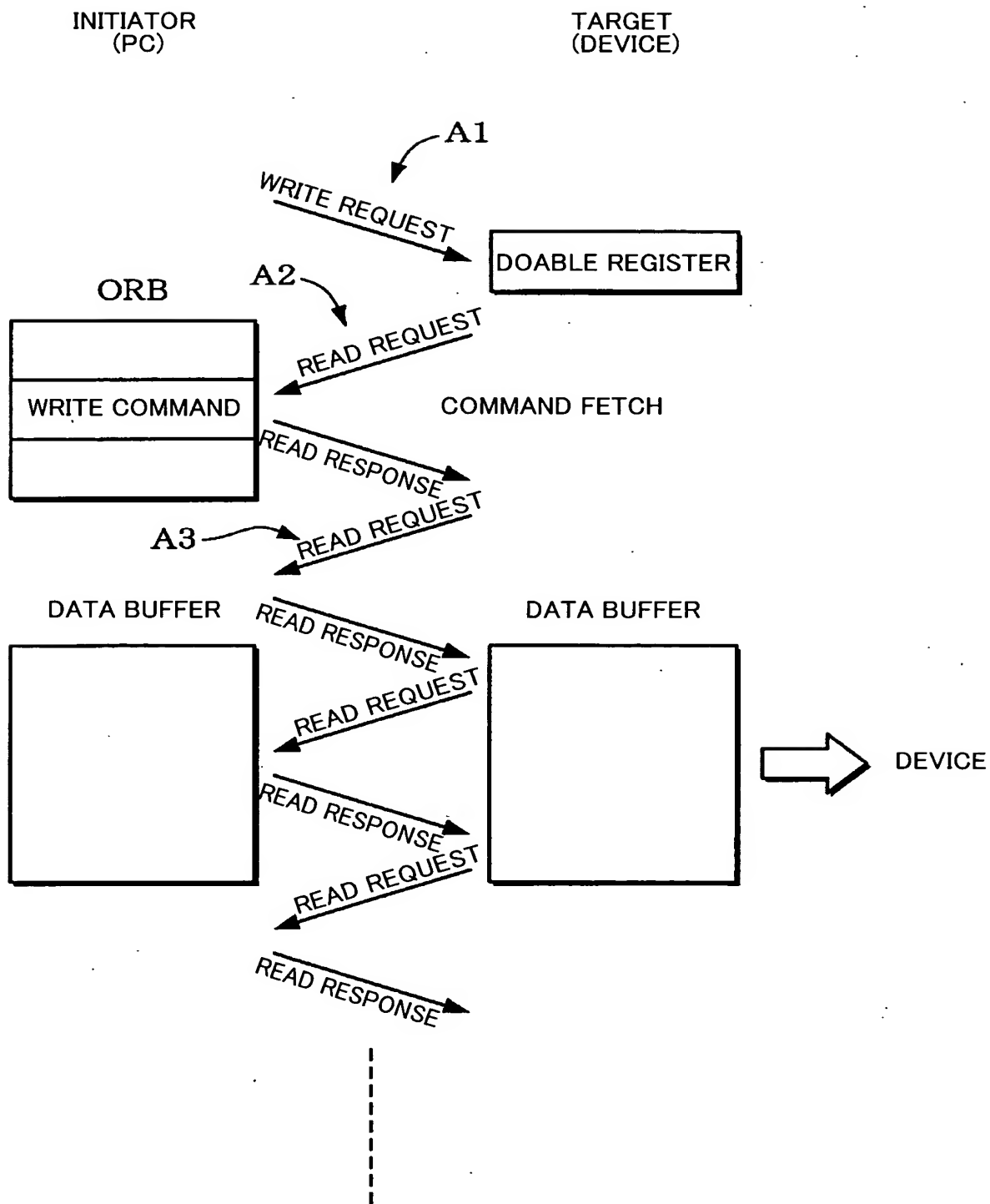


FIG. 4

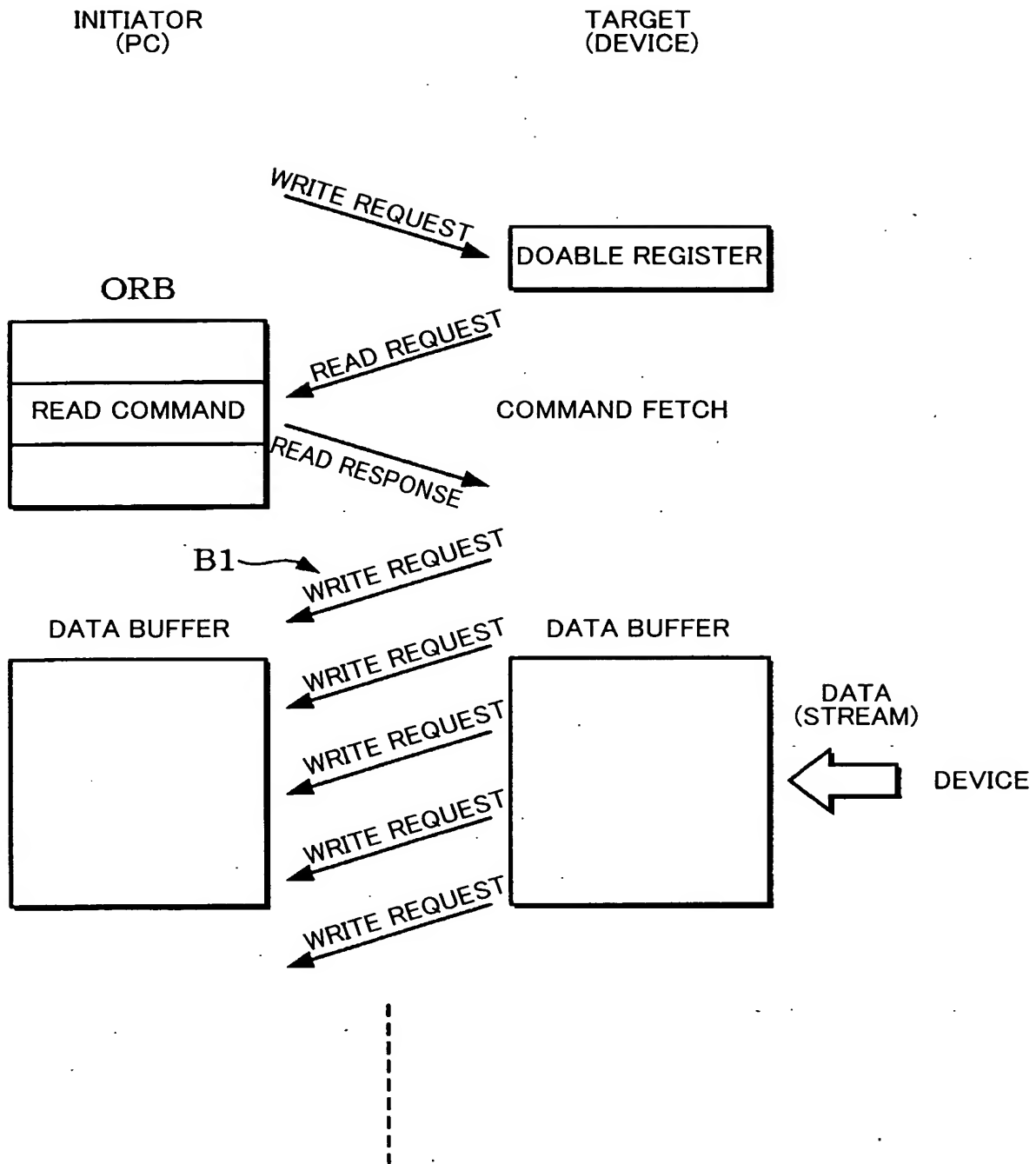


FIG. 5A

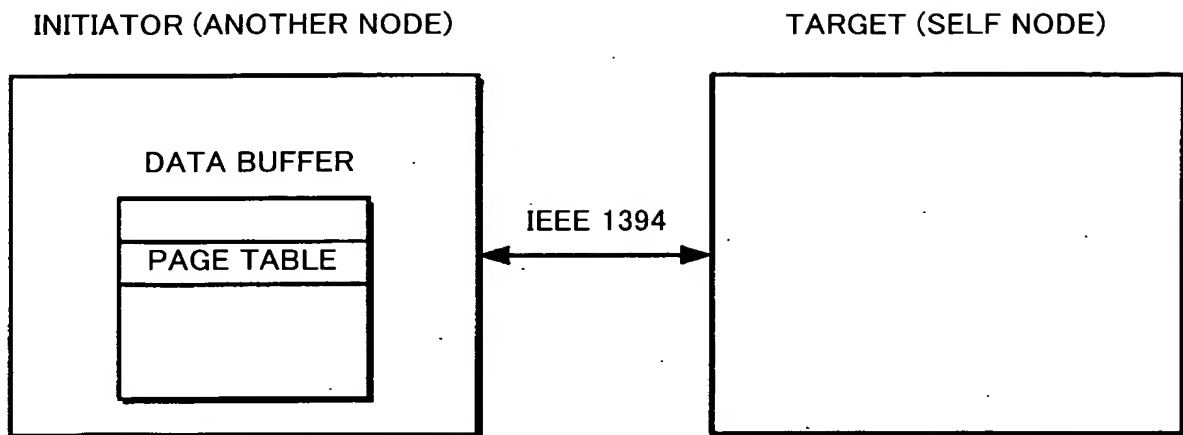


FIG. 5B WHEN PAGE TABLE IS PRESENT

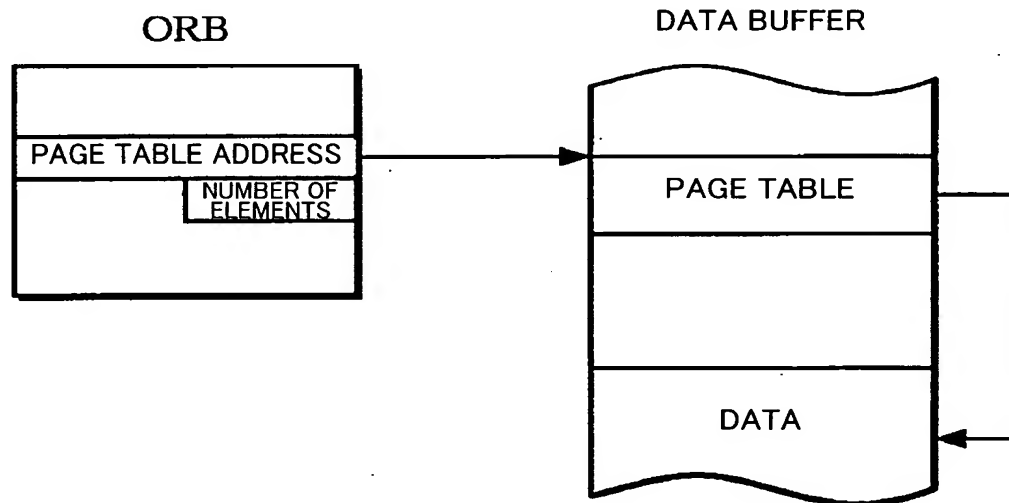


FIG. 5C WHEN PAGE TABLE IS ABSENT

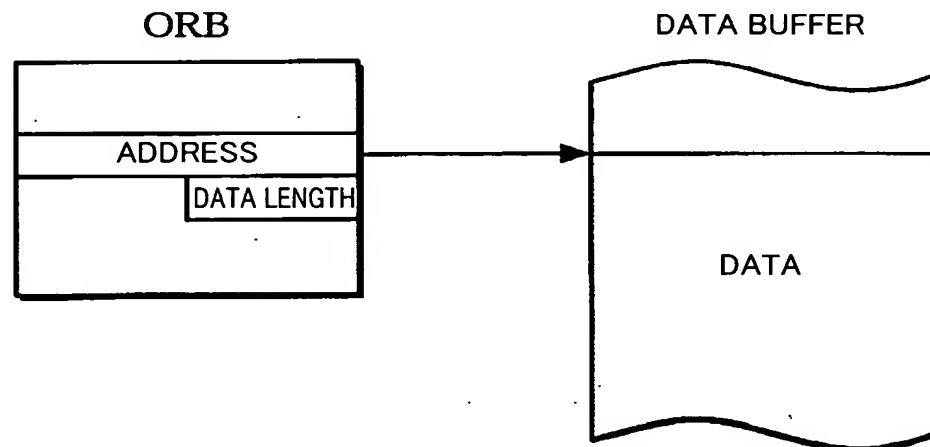


FIG. 6A

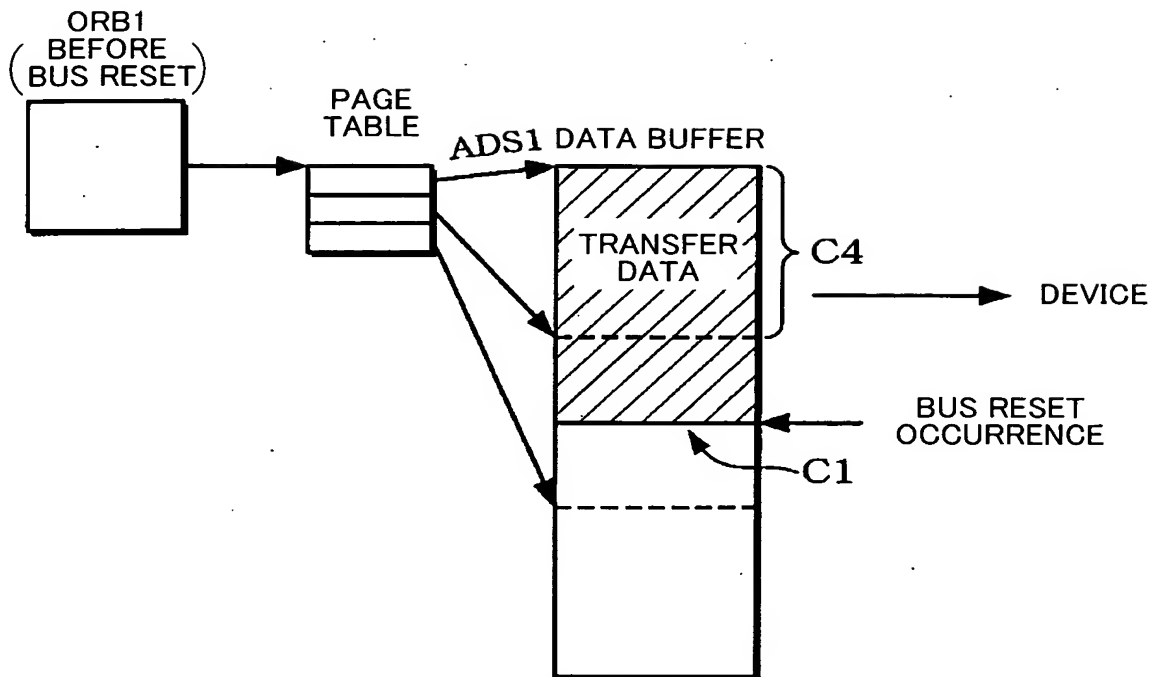


FIG. 6B

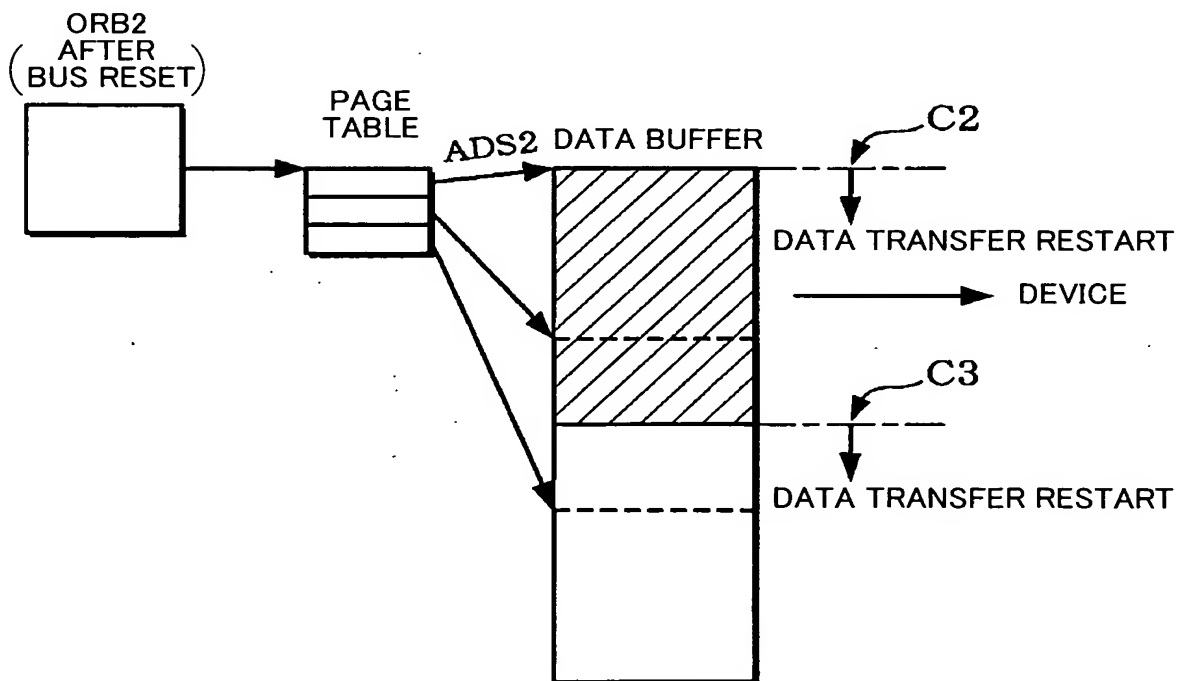


FIG. 7

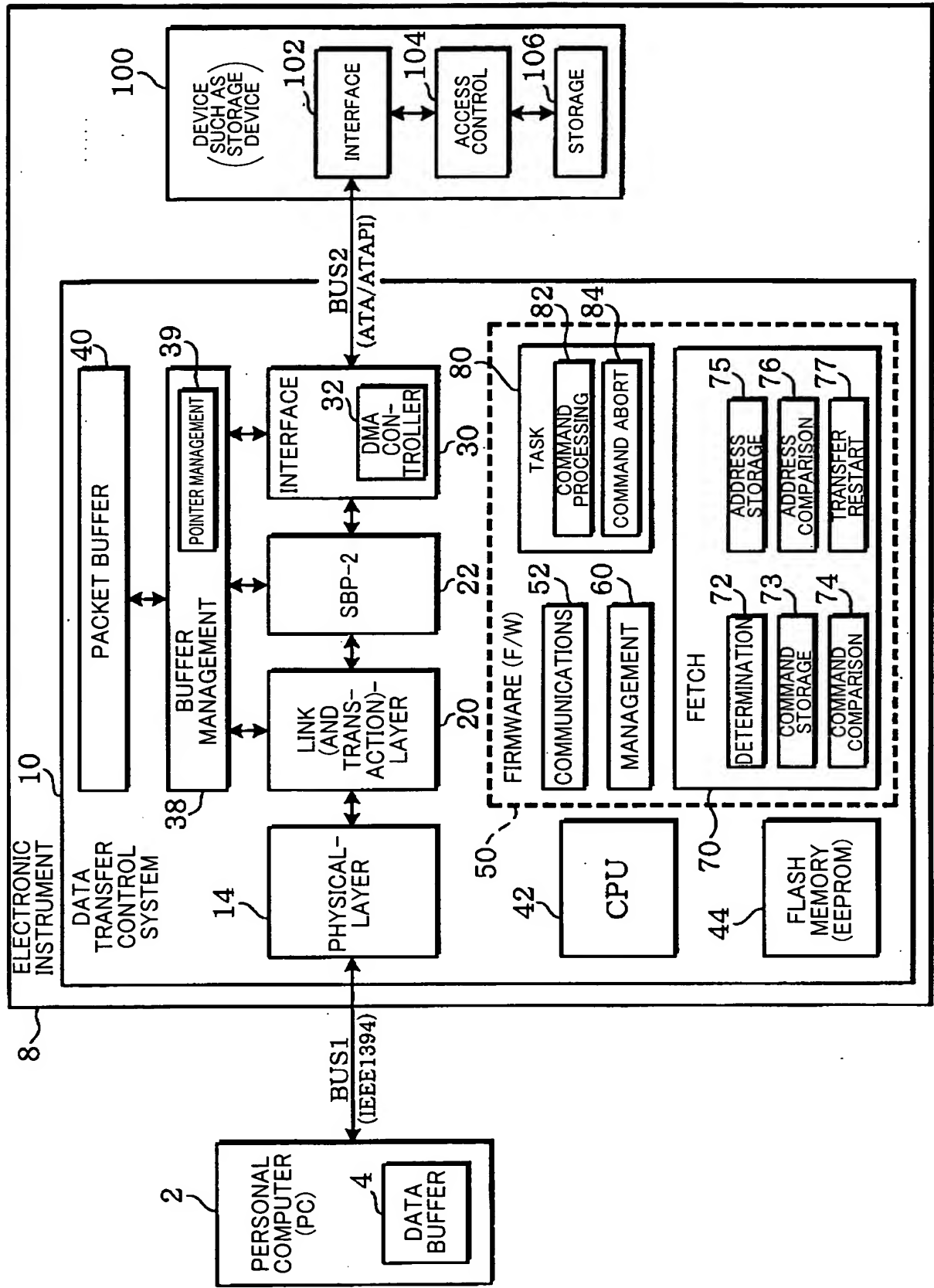


FIG. 8

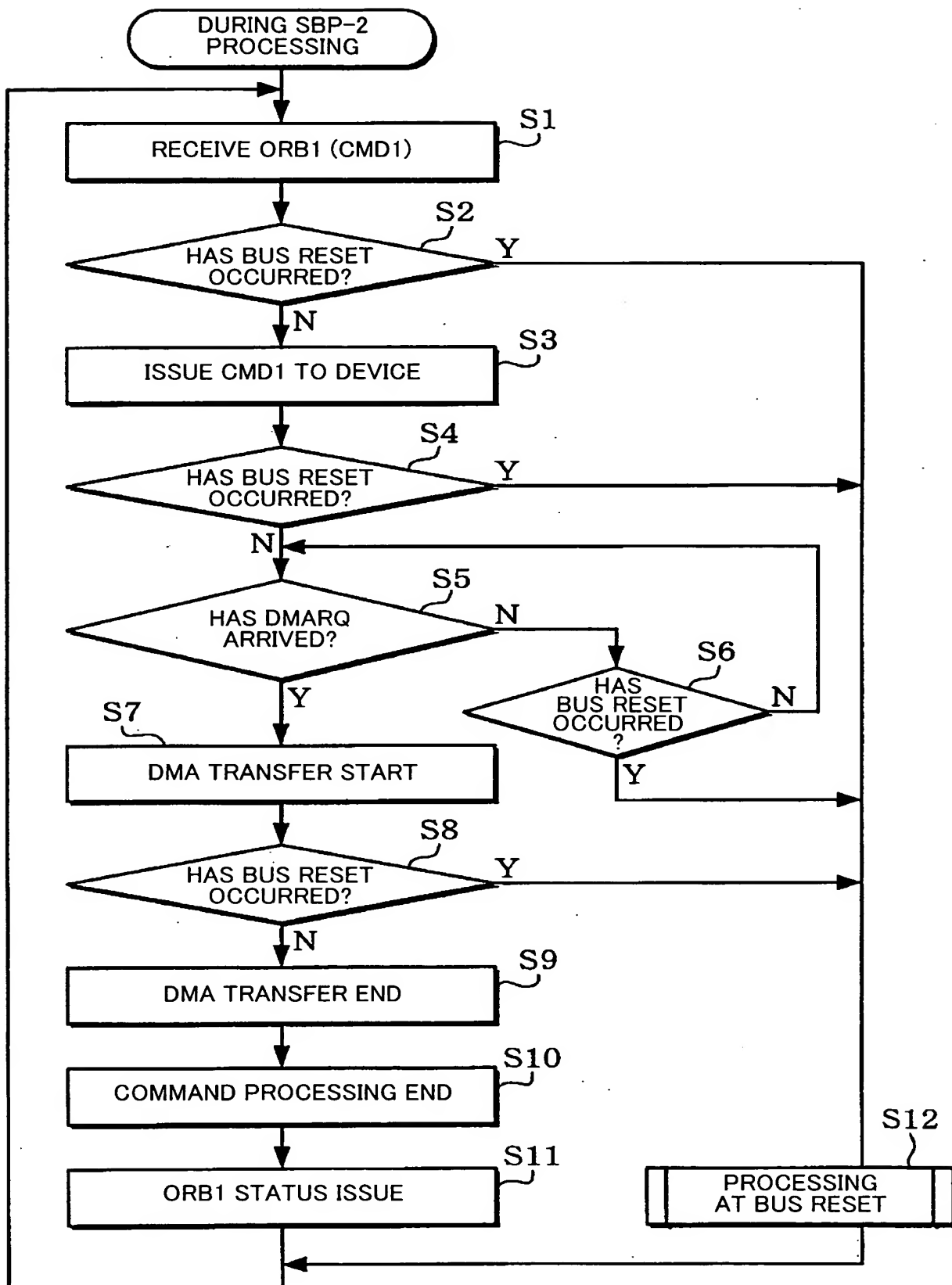




FIG. 9

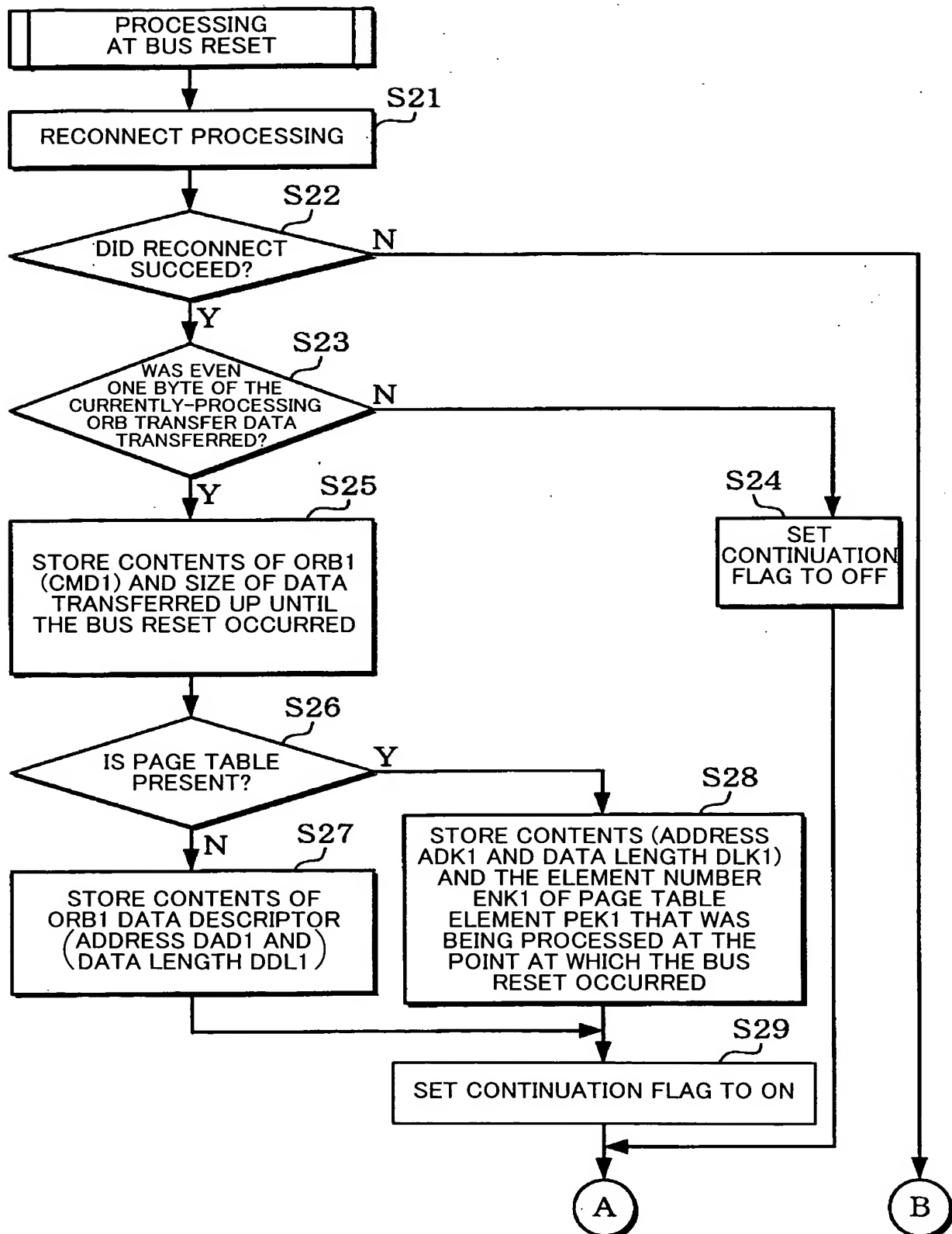


FIG. 10

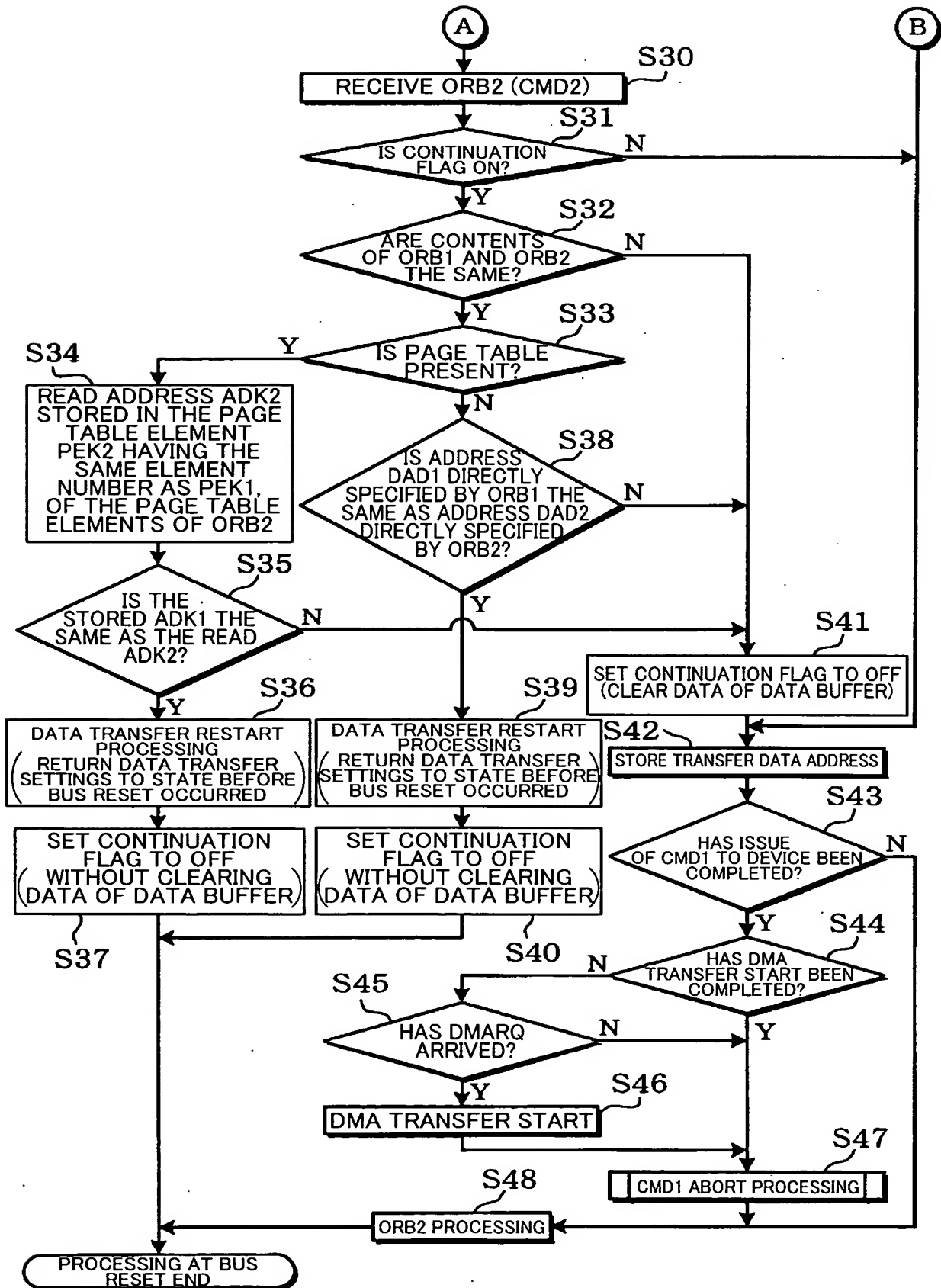


FIG. 11

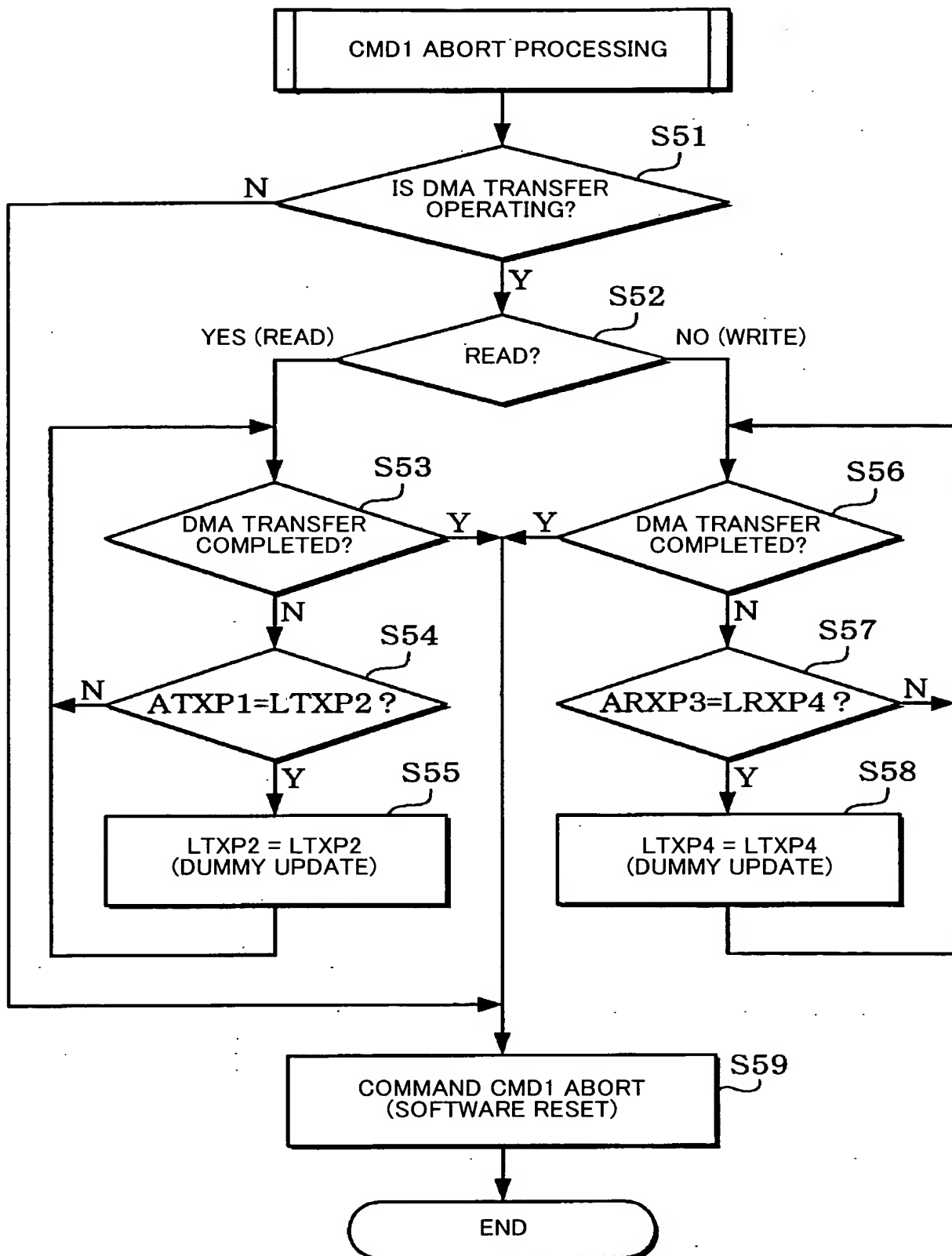


FIG. 12

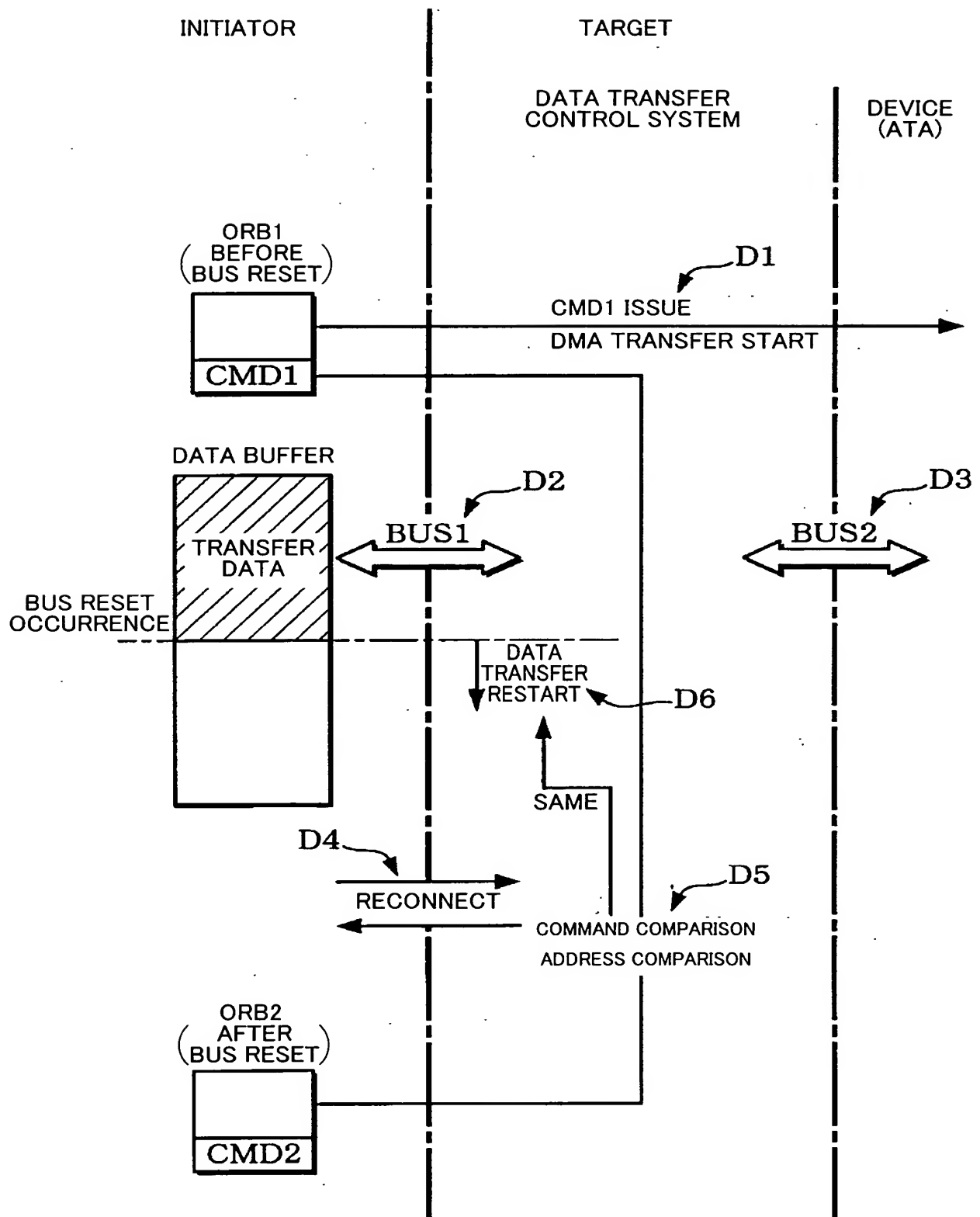


FIG. 13

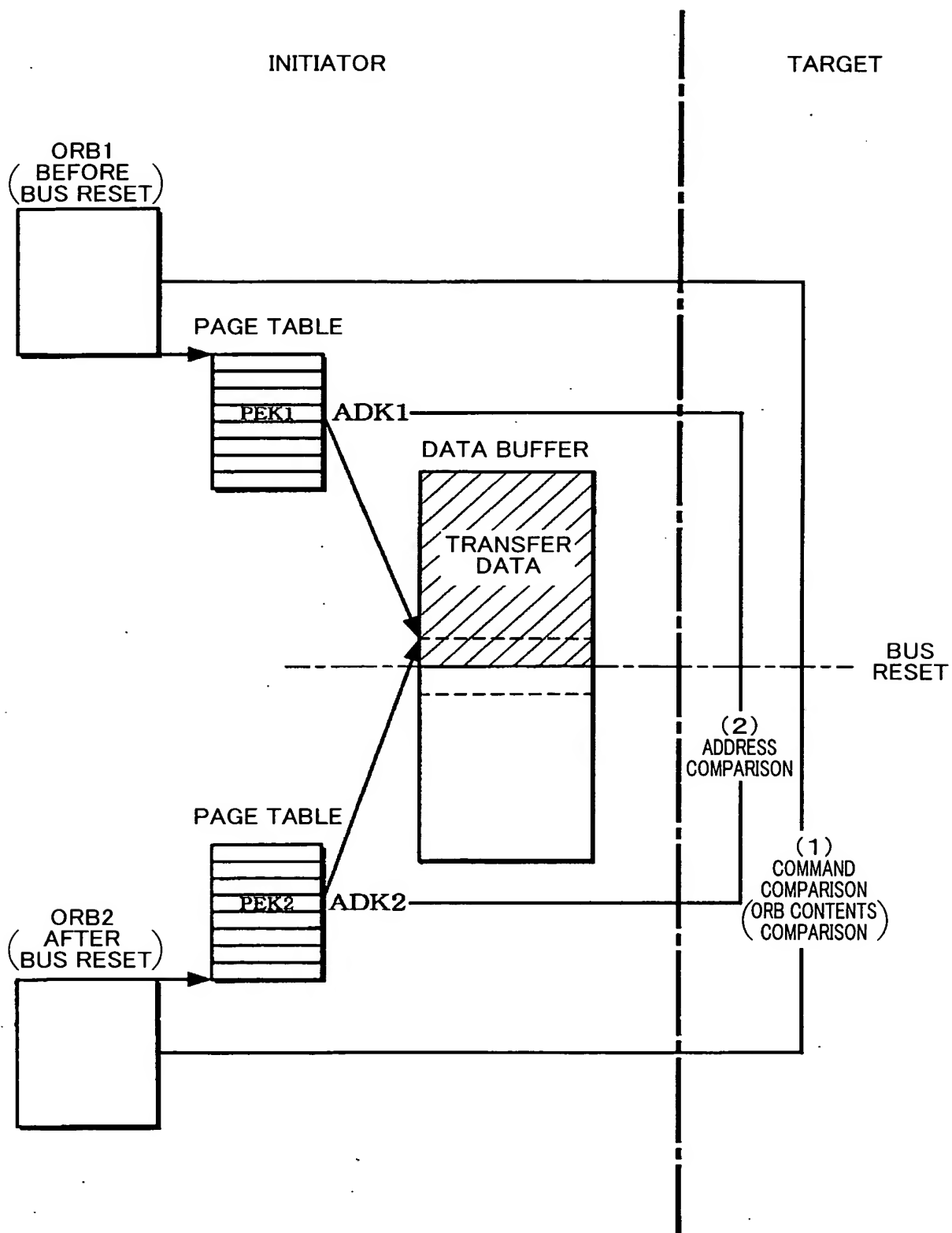


FIG. 14

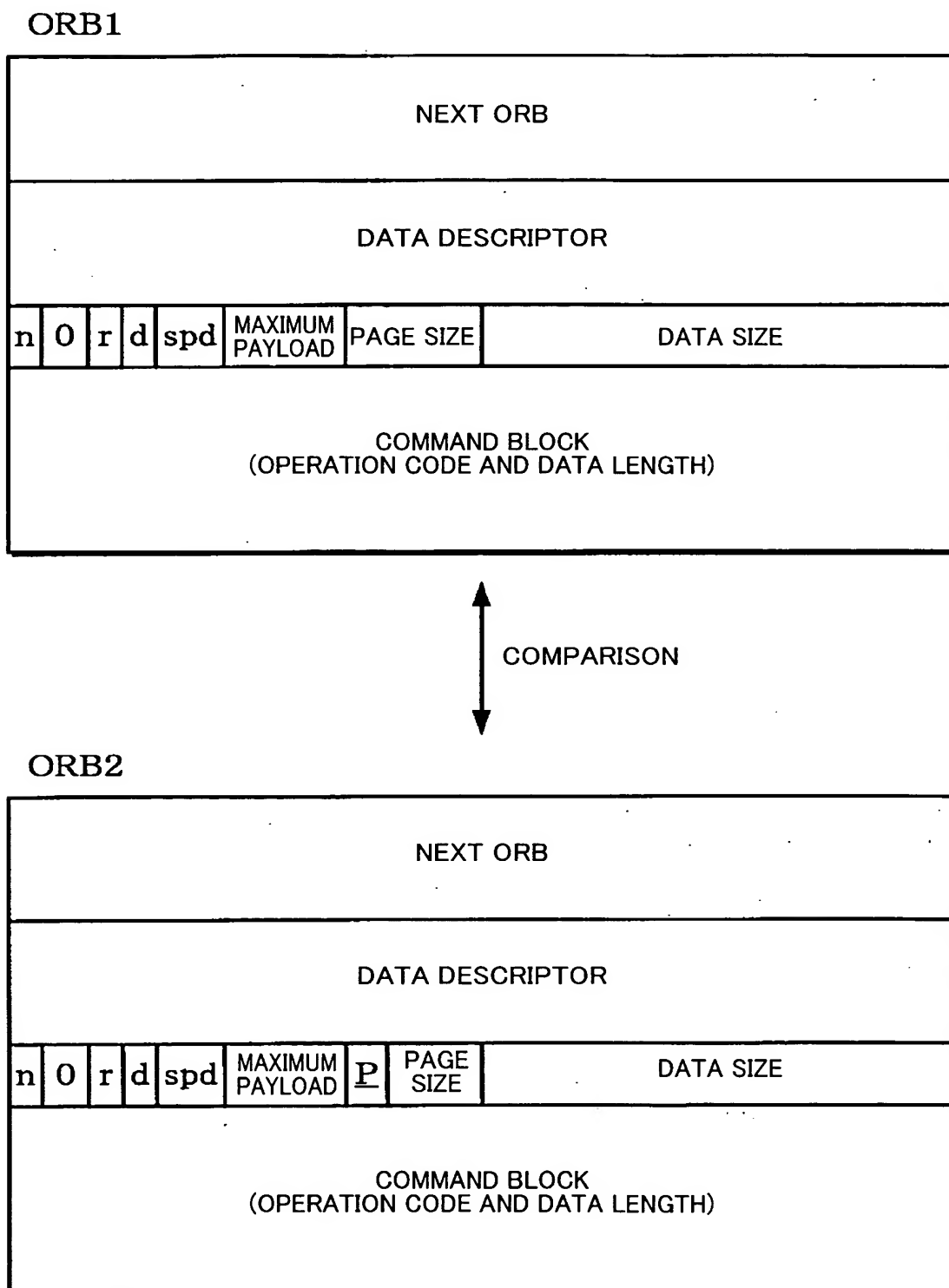


FIG. 15

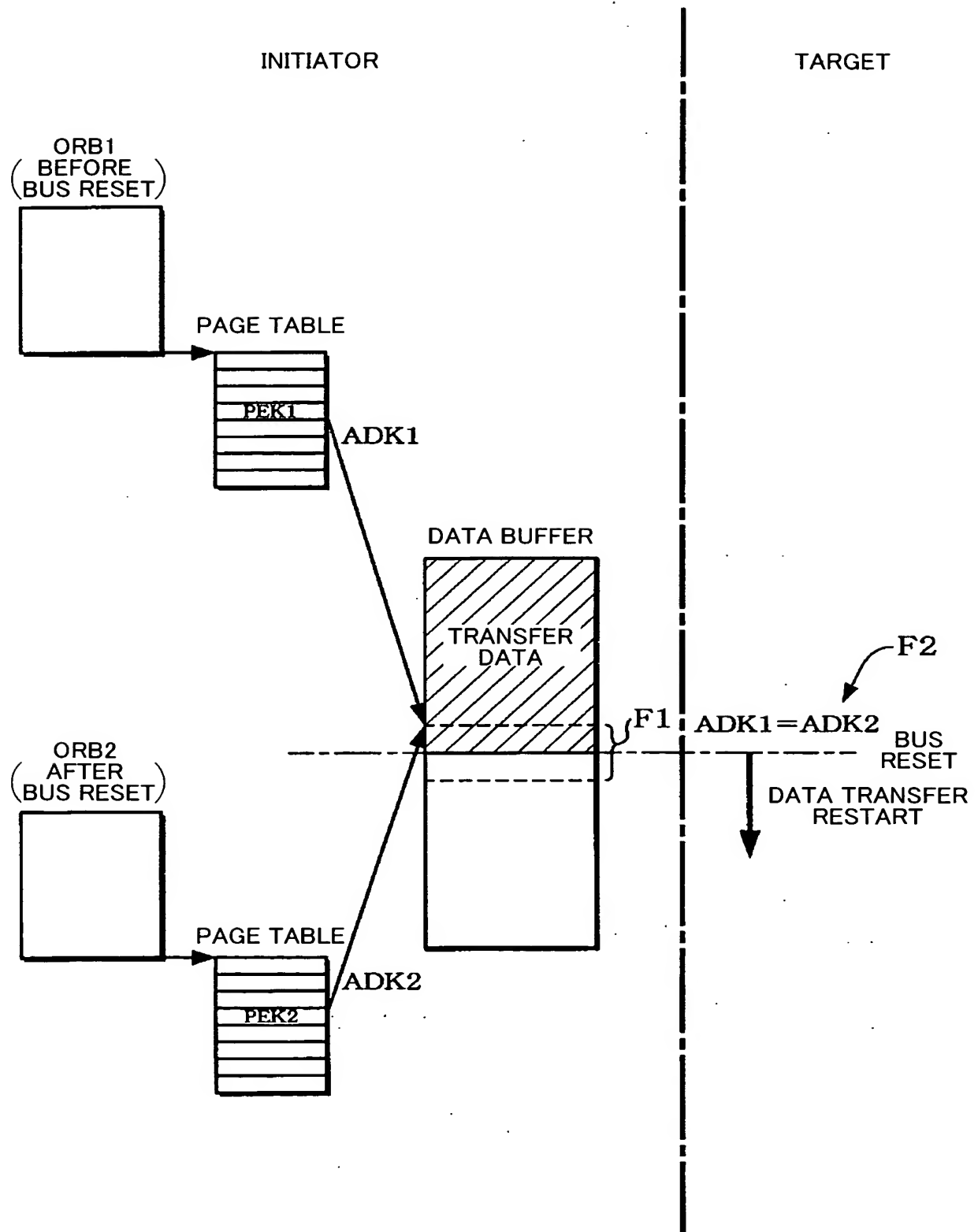


FIG. 16

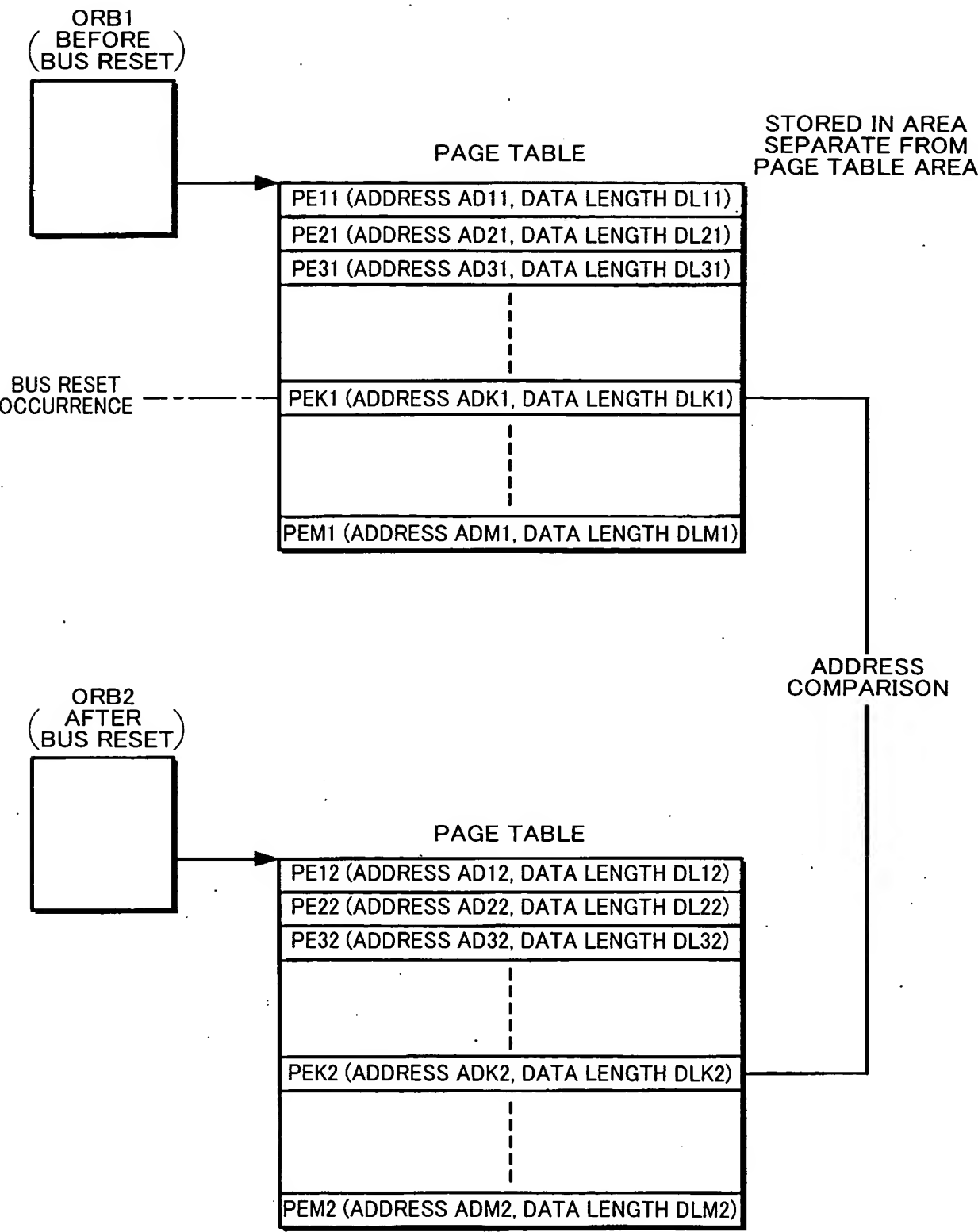




FIG. 17

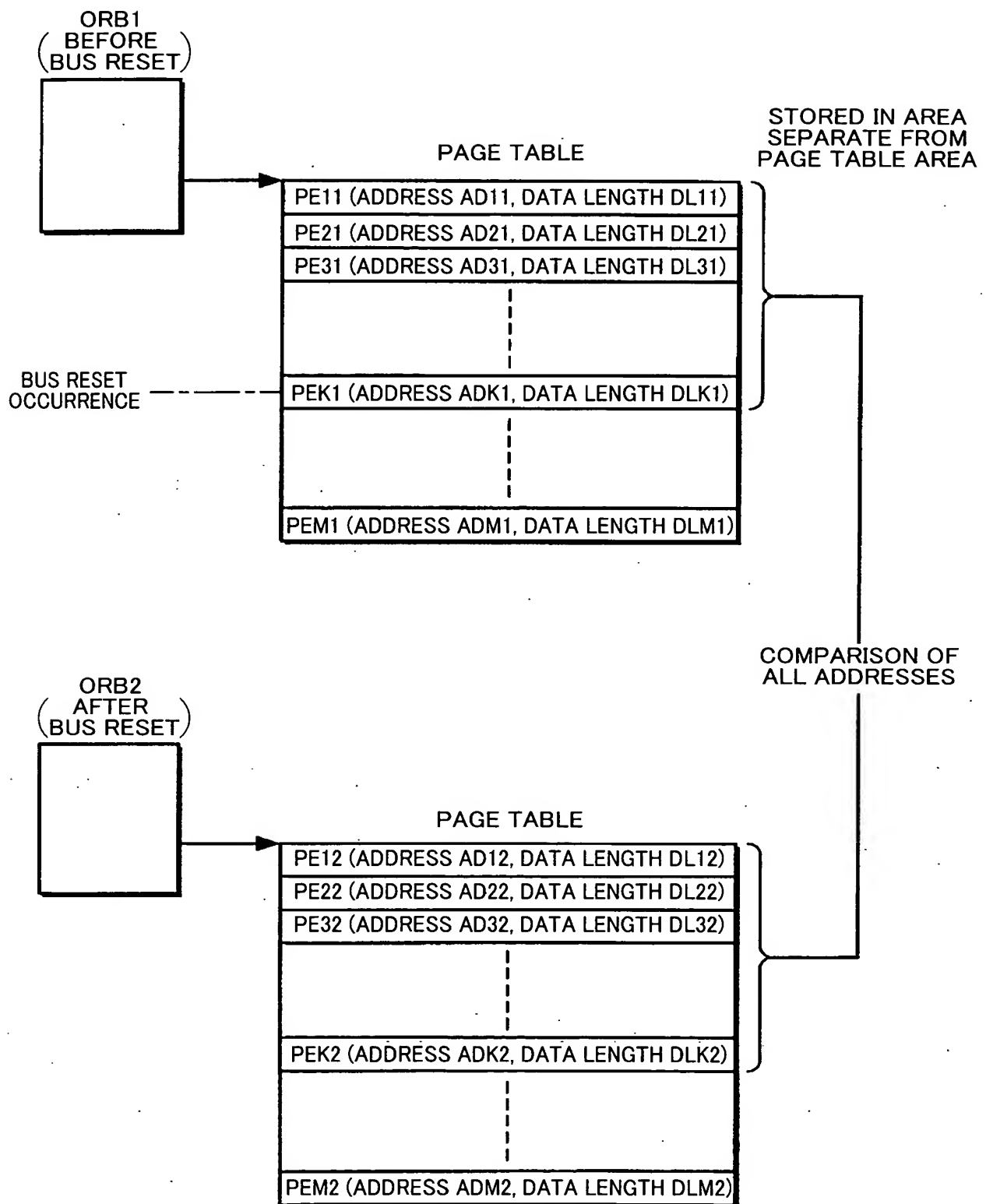


FIG. 18

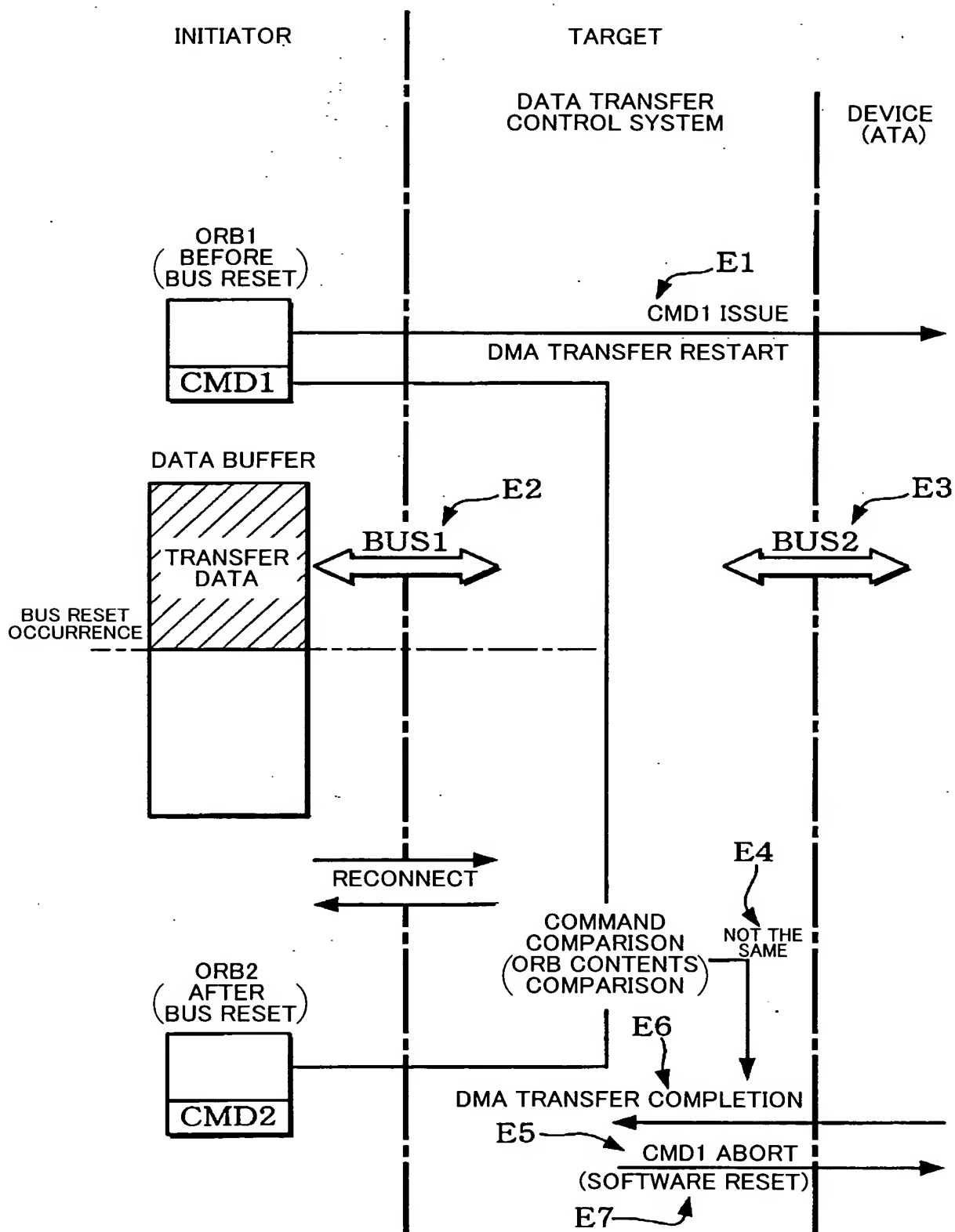




FIG. 20A

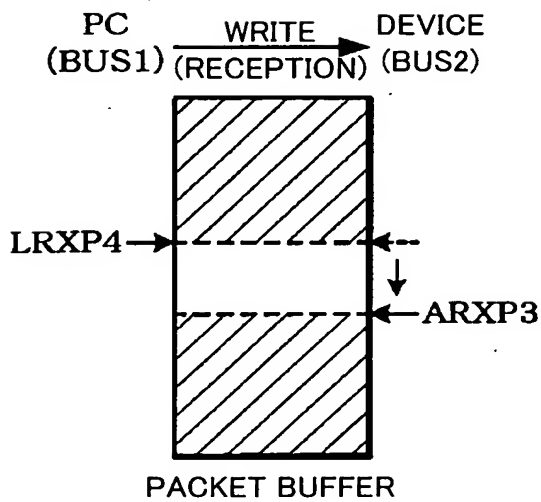


FIG. 20B

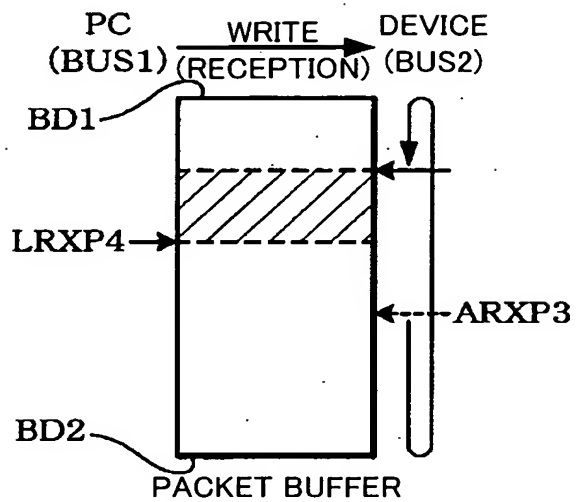


FIG. 20C

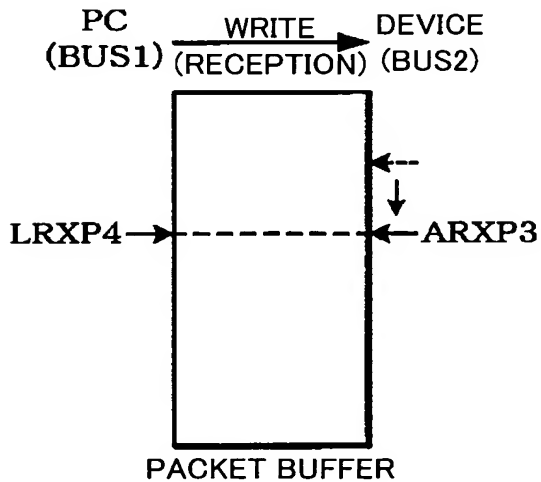


FIG. 20D

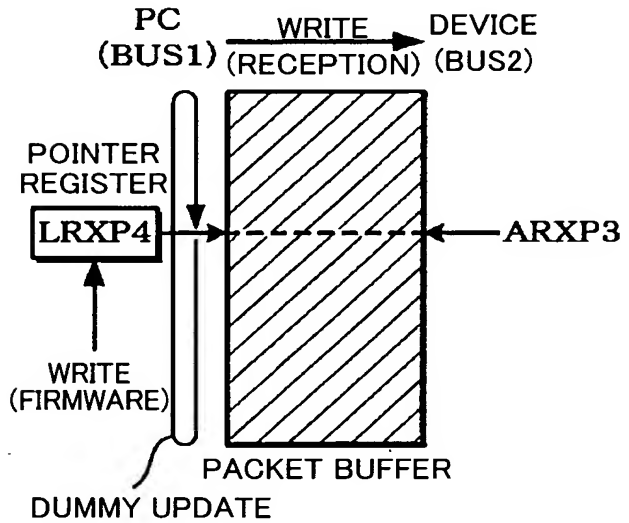


FIG. 20E

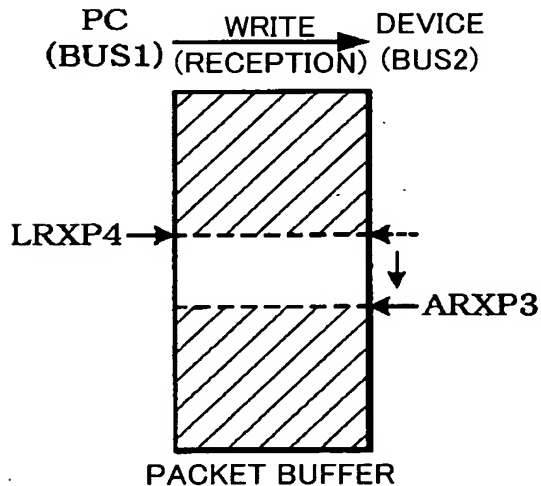
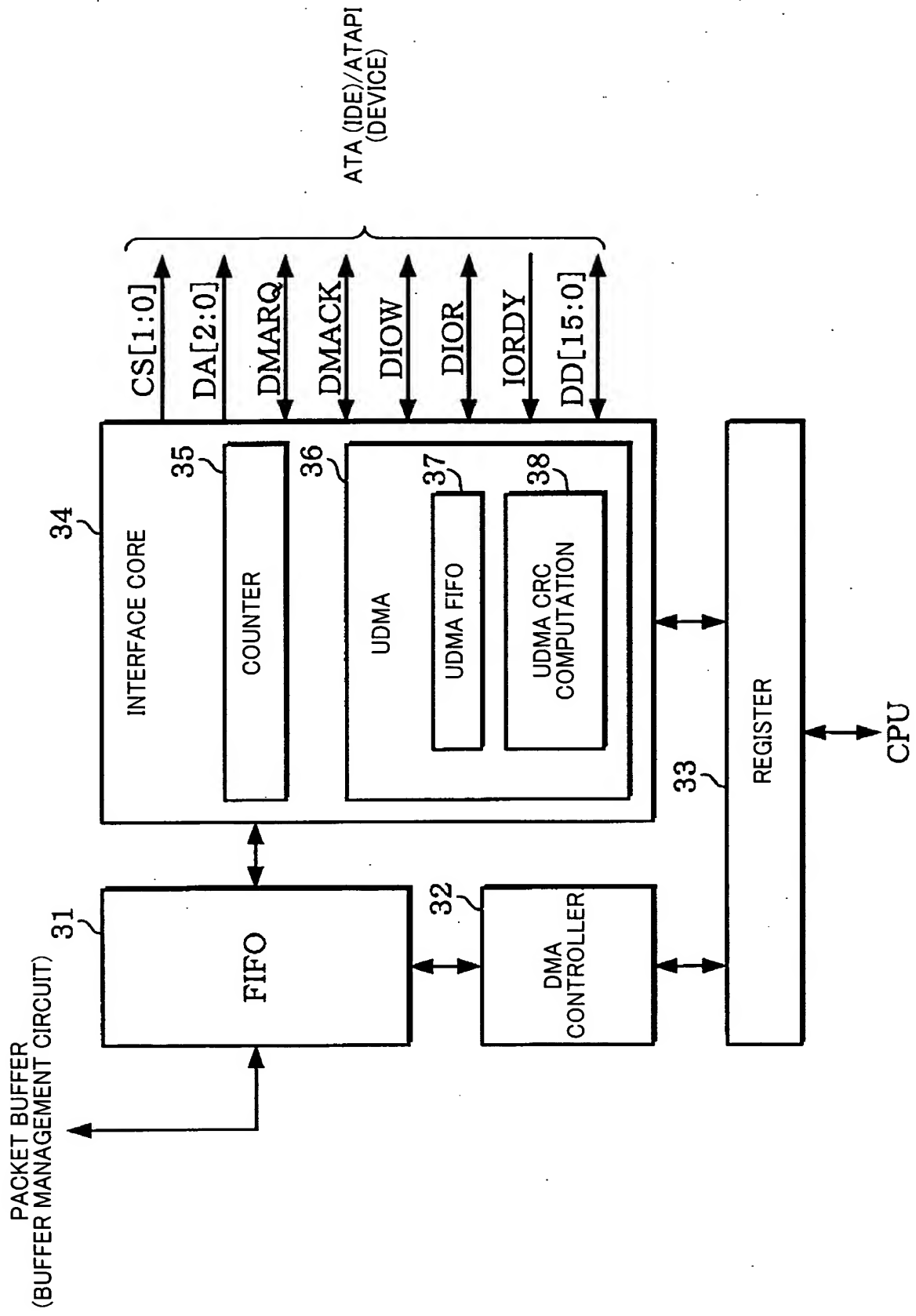
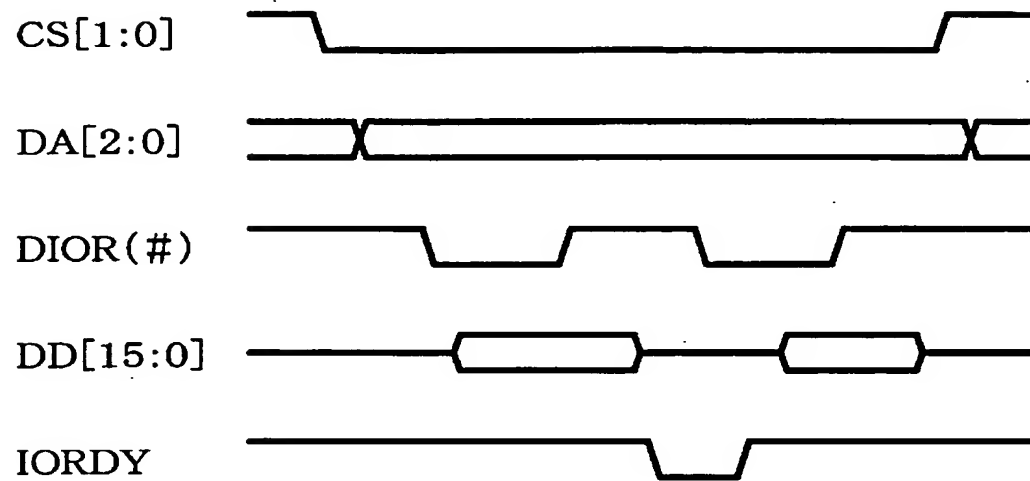


FIG. 21



**FIG. 22A** PIO READ (DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)



**FIG. 22B** PIO WRITE (PC → DATA TRANSFER CONTROL SYSTEM → DEVICE)

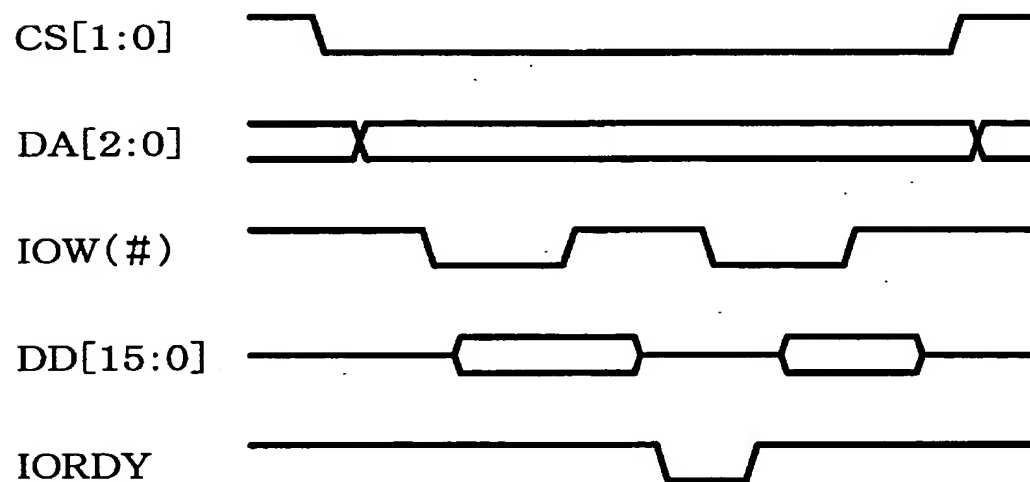


FIG. 23A DMA READ (DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)

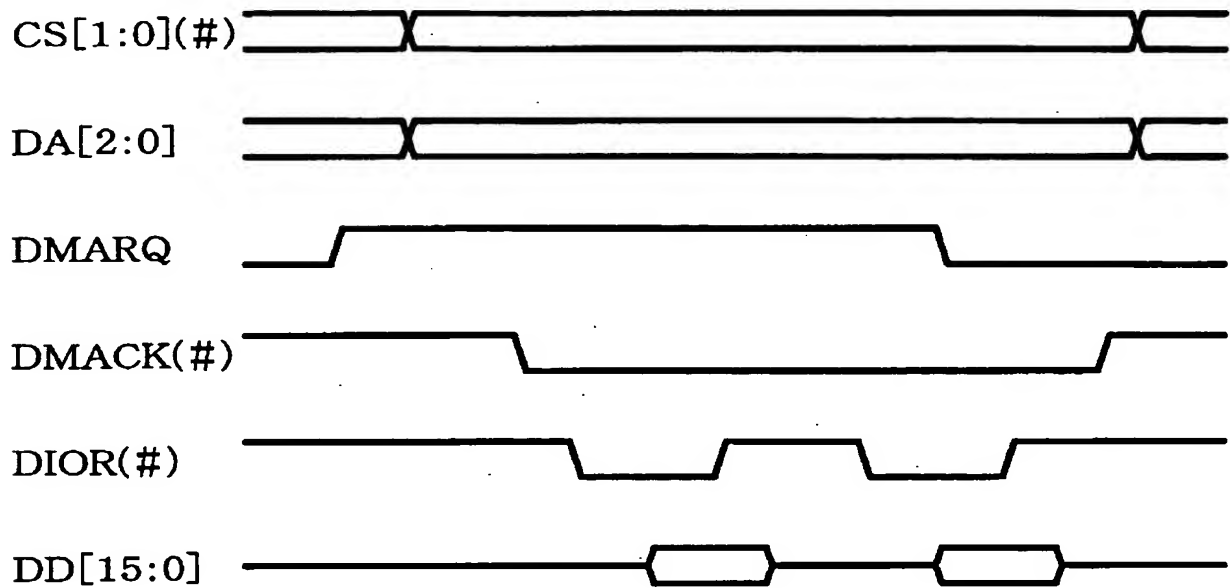


FIG. 23B DMA WRITE (PC → DATA TRANSFER CONTROL SYSTEM → DEVICE)

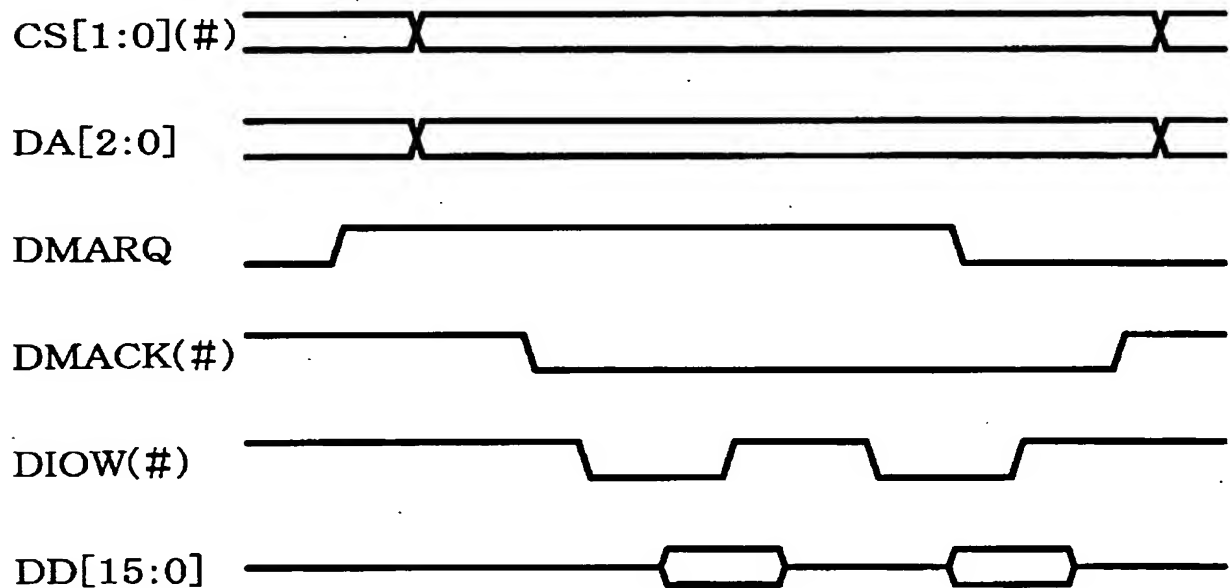


FIG. 24A

ULTRA-DMA READ (DEVICE → DATA TRANSFER CONTROL SYSTEM → PC)

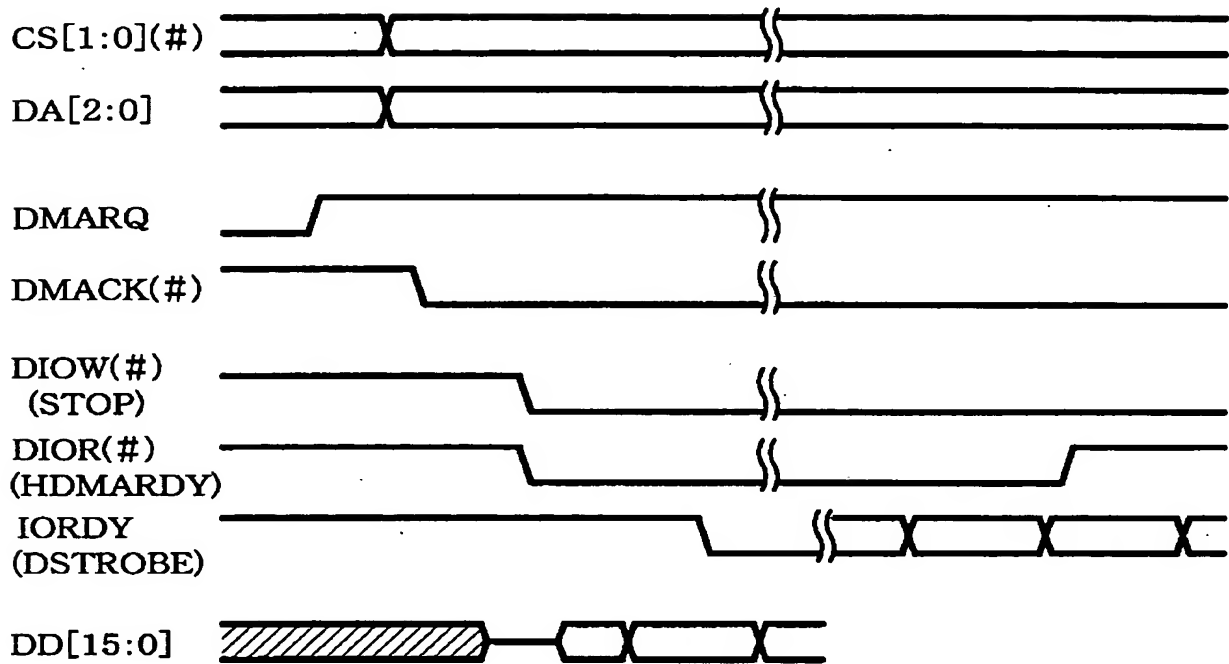


FIG. 24B

ULTRA-DMA WRITE (PC → DATA TRANSFER CONTROL SYSTEM → DEVICE)

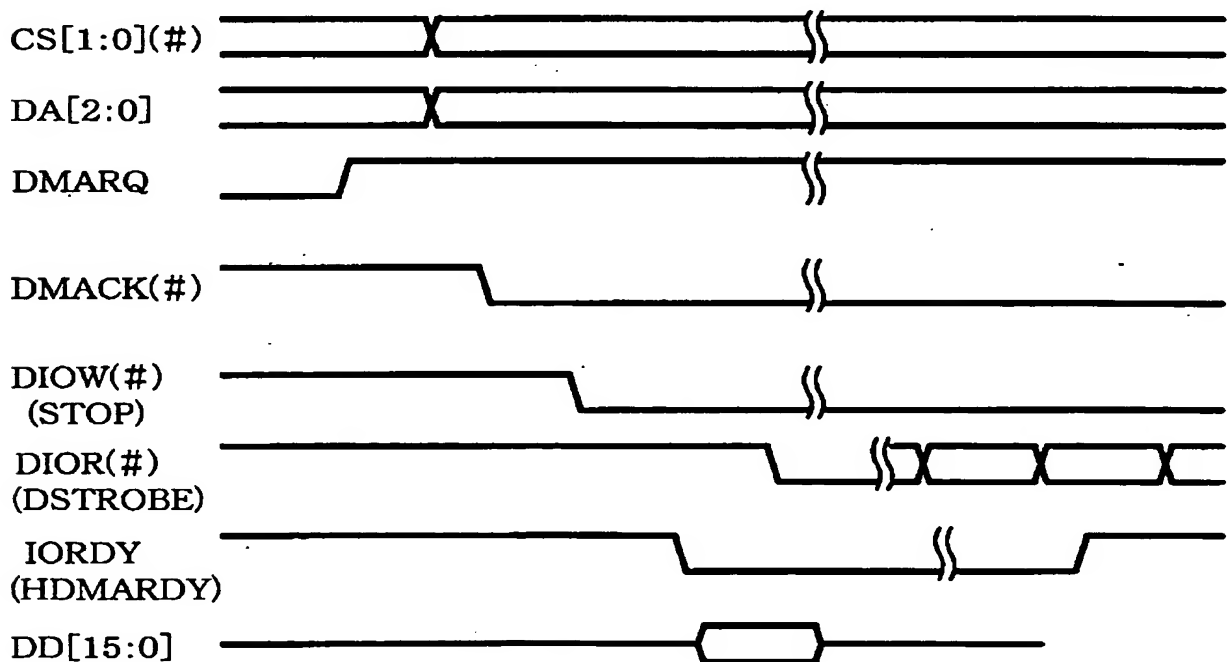




FIG. 25

